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September 29, 2006
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APPLICATION NO.	10/724,299
FILING DATE	11/26/2003
FIRST NAMED INVENTOR	Raffi Codilian
ART UNIT	2841
CONFIRMATION NO.	1174
EXAMINER	Yuriy Semenenko
ATTORNEY DOCKET NO.	A1398

TITLE	DISK DRIVE PRINTED CIRCUIT BOARD WITH COMPONENT-DEDICATED ALIGNMENT LINE INDICATORS INCLUDING INNER AND OUTER LINE SEGMENTS AND METHOD OF PRODUCING A PRINTED CIRCUIT BOARD ASSEMBLY

ATTACHED WITH THIS SUBMISSION:

1. Notice of Appeal (1 page)
2. Pre-Appeal Brief Request for Review, form PTO/SB/33 (5 pages)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 10/724,299	Confirmation No.: 1174
Application of Raffi Codilian	Art Unit: 2841
Filed: November 26, 2003	Examiner: Yuriy Semenenko
For: DISK DRIVE PRINTED CIRCUIT BOARD WITH COMPONENT-DEDICATED ALIGNMENT LINE INDICATORS INCLUDING INNER AND OUTER LINE SEGMENTS	Attorney docket: A1398

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

In response to the Final Office Action mailed June 30, 2006 and the Advisory Action mailed August 30, 2006, Applicant requests that the claim rejections be reviewed prior to the filing of an Appeal Brief for the reasons provided below.

Issues for Review

Applicant believes there are clear errors in the Examiner's rejections that should be reviewed and that such a review will show that the cited references do not support a rejection of the pending claims.

Briefly, a clear error exists in the Examiner's rejections because the Examiner has failed to show that the cited references teach or suggest all the limitations of the pending claims. The Applicant has pointed out specific claim limitations that are not shown by the references, but the Examiner's answers in the Final Office Action and in the Advisory Action have explained how and where he believes the limitations are shown by the cited references but instead consist of an unsupported statement that the prior art structure is capable of performing the intended use. Applicant asserts that the Examiner has not met his burden of properly stating a *prima facie* case of anticipation or of obviousness for the pending claims.

Claims 1-4 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. Appl. Publ. No. 2002/0050397 ("Sakamoto"). The following discussion is provided to explain why Applicant believes the Examiner has committed an error that should be reviewed by a panel prior to the filing of an Appeal Brief.

Sakamoto does not teach or discuss alignment of electrical components on a printed circuit board. Instead, Sakamoto discusses a method for better controlling the temperature of a semiconductor module on a flexible sheet of a disk drive. This is a very different problem than that addressed by Applicant, and Sakamoto does not discuss accurate aligning but teaches instead enhanced heat dissipation. To this end, Sakamoto shows in Figs. 1A, 1B, 2A, 2B, and 2C a flexible sheet 11 made up of two insulating sheets P1 and P2 between which pad electrodes PD are sandwiched. A first opening OP is cut in the sheet P2 to expose the pads PD and a hole 13 is cut through both sheets P1 and P2. A semiconductor module 10 is mounted on the flexible sheet 11 with a portion contacting the pads PD and a portion extending through the hole 13 to mate with a radiation substrate 13A.

In contrast to Sakamoto, claim 1 calls for "component-dedicated alignment indicators" disposed on the mounting surface of a circuit board body. Sakamoto fails to teach any "indicators visibly disposed at the mounting surface" as called for in claim 1. The Examiner cites Sakamoto in Fig. 1 and its "circuit board 11" as showing these indicators for use with component 10. As seen in Figs. 1A, 1B and 2A, Sakamoto teaches a flexible sheet 11 that includes no visible indicators on its surface for aligning component 10. Instead, Sakamoto teaches that an opening OP is cut through its insulating sheet P2 and another opening 13 is cut through another insulating sheet P1. There are no alignment lines provided on the surface of sheet P2 but instead in Fig. 1A it is shown that the component 10 is mounted to the surface of sheet P2 exterior to opening OP (e.g., see dashed lines indicating where component 10 would be mounted on the surface of sheet P2). As can be seen clearly in Fig. 1A, there are no visible alignment line indicators provided on flexible sheet 11. As a result, the Examiner has failed to cite a reference that includes each and every limitation of claim 1.

The Response to Arguments in the Final Office Action of June 30, 2006 provides no response to this argument, but, instead, it simply restates the prior rejection of claim 1. In this rejection, the Examiner presents his own Fig. 1 and Fig. 2 that correspond generally to Sakamoto's Figs. 2A and 2C, respectively. Fig. 1 is used to assert that the first and second outer line segments are shown by the edges of the flexible sheet 11. However, these are physical edges of the board and are not "visibly disposed at the

mounting surface." Fig. 1 provides a solid line that is used to show the measurements of first and second inner spacings. However, this line is shown dashed in Fig. 2A of Sakamoto as it represents the hidden outer sides or edges of component 13A, which according to para. [0123] of Sakamoto is a radiation substrate. This radiation substrate 13A is mounted on the flexible sheet 11 on the opposite side of the flexible sheet 11 relative to semiconductor device 10. Hence, the solid line shown in the Examiner's Fig. 1 is not actually present as a visibly disposed line on a mounting surface of sheet 11, and, as a result, the indicator lines of claim 1 are not shown in the Examiner's Fig. 1 or in Sakamoto's Fig. 2A. Hence, the modification of the references figures in an attempt to find each limitation of the claims is a clear error for review.

Fig. 2 provided by the Examiner points to layer P2 of Sakamoto and to the edge of device 10 as showing the "Component-dedicated alignment line indicator." These cited features are different than the solid line shown in the Examiner's Fig. 1, but these features also fail to show "visibly disposed" line indicators "at the mounting surface" as called for in claim 1. Specifically, the side of the device 10 itself is not on the mounting surface (until the device is mounted) and would not assist in alignment without additional visibly disposed indicators. The layer P2 also fails to show the visibly disposed line indicators. Fig. 1A of Sakamoto shows that layer P2 of sheet 11 provides the mounting surface for the device 10, and this can be seen by dashed lines that show that the corners of device 10 rest on the layer P2 with the recessed surface OP below it (such mating of device 10 and the upper surface of layer P2 is further shown in Sakamoto in Fig. 2B). As can be seen, layer P2 provides the mounting surface, but, as shown in Fig. 1A of Sakamoto, there are no visibly disposed line indicators, and the edge of OP cannot reasonably be said to be a line indicator visibly disposed on the mounting surface of layer P2. The only alignment shown by Sakamoto is that the device 10 should be mounted with its corners outside the OP on an upper or mounting surface of layer P2, but such alignment is not achieved with the assistance of any visibly disposed line indicators at the surface of sheet 11. For these additional reasons, Sakamoto fails to teach or suggest the disk drive printed circuit board of claim 1, and Applicant believes the Examiner has made a clear error in rejecting the claim.

In addition to the requirement that the line indicators be visibly disposed on the mounting surface, claim 1 calls for first, second, third, and fourth line segments in the line indicators on the mounting surface of the board, with the distance between opposing pairs of the lines being based on the electrical component. These four lines are not shown on the surface of 11 (i.e., on either the sheet P1 or sheet P2). The Office Action provides a "Fig. 1" that is a marked up version of Sakamoto's Fig. 2A. As discussed in the prior Amendment, Applicant disagrees with the Office Action's construction of Sakamoto's Fig. 2A provided in the Office Action's Fig. 1. Specifically, the Office Action's Fig. 1 is labeled such that apparently the four inner lines are shown by a rectangle that has "first inner spacing" and "second inner line spacing." However, as discussed above, it appears that this rectangle coincides with the dashed lines in Sakamoto's Fig. 2A that show the radiation substrate 13A. The radiation substrate 13A is shown in dashed lines in Fig. 2A because it is hidden from view and is not provided on the surface of flexible sheet 11. There are no lines "visibly disposed" on the mounting surface of flexible sheet 11 that can be said to teach the four inner line segments called for in claim 1. For this additional reason, Sakamoto fails to anticipate the printed circuit board of claim 1. The Response to Arguments failed to rebut this argument, and Applicant requested that the rejection be withdrawn as unsupported or that the Examiner indicate specifically where in Sakamoto's figures (without additions or modifications) the four inner line segments are shown or described.

Additionally, claims 5, 6, and 16-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sakamoto in view of U.S. Pat. No. 6,798,609 ("Bonin"). Independent claim 16 includes limitations similar to claim 1, and the reasons provided for allowing claim 1 over Sakamoto are believed equally applicable to claim 16.

As discussed below with reference to claims 5 and 6, Bonin fails to overcome the deficiencies of Sakamoto discussed with reference to claim 1. Claim 16 also calls for the inner line segments disposed upon the mounting surface to define a rectangle at least as large as the base of the electrical component. The Office Action cites Fig. 1 provided in the Office Action, but as discussed above, the only rectangle cited is the outline of component 13A which is not on the mounting surface of sheet 11, and as a result cannot show the four inner line segments of claim 16. For these reasons, claim

16 and claims 17-20, which depend from claim 16, are not shown or suggested by the combined teaching of the two cited references.

Claims 5 and 6 depend from claim 1 and, as a result, the reasons provided for allowing claim 1 over Sakamoto apply equally to claims 5 and 6. In the Office Action, Sakamoto is described as failing to show the component-dedicated alignment line indicators that include fourth outer line segments with the characteristics called for in claims 5 and 6, and Bonin is cited as overcoming these deficiencies in the base reference. However, Bonin fails to overcome the deficiencies of Sakamoto.

Specifically, Bonin fails to show any visibly disposed indicator lines on its mounting surfaces. The Office Action cites Bonin with reference to Fig. 3 and the beams 33 and 35, but there is no discussion in Bonin regarding providing four inner indicator lines having a particular spacing and then providing two outer line segments. Hence, the combined teaching of Sakamoto and Bonin would not provide the circuit board of claim 1. Claim 5 calls for third and fourth outer line segments and neither Sakamoto nor Bonin provide such teaching. The Examiner asserts this is taught by "any lines close to a disk drive electrical components" such as beams 33 and 35. However, there is no teaching these are provided as alignment indicators or that they would be useful for such a purpose but are instead described as being deformable connectors for connecting inner frame 40 to outer frame 38 in lines 59-67 of col. 2. The beams 33 and 35 fail to teach the third and fourth indicator lines of claims 5 and 6 (and where would the first and second indicator lines be in Bonin?). The Response to Arguments and Advisory Action failed to address these arguments distinguishing claims 5 and 6 from Bonin. For these reasons, Applicant requests that the rejection of claims 5 and 6 be reviewed.

Conclusions

Applicant respectfully requests that a panel review the Examiner's rejections for clear error and provide a finding that prosecution should be reopened.

Respectfully submitted,

September 28, 2006

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